天下智联®

产品承认书

SPECIFICATION FOR APPROVAL

客户 Customer：_____

产品名称 Model Name：16 Port 100M Switch

产品编号 Model number：TXE102

日期 Date:_____

SIGNATURE:

业务 SALES	工程 ENG	制造 MFG	品质 QUALITY
APPROVED BY	CHECKED BY	CHECKED BY	TESTED BY

CUSTOMER APPROVAL:

CUSTOMER APPROVAL BY	
DATE	

1、 Product Photo

Front:

Back:

2、Product specification

Model number	TXE102
Chipset	IP1717B
Port number	16 port 10/100M Auto MDI-MDIX RJ45
Standard	IEEE 802.3、IEEE 802.3u、IEEE 802.3x、IEEE 802.3az
Network media	10Base-T,cat3 or above UTP,10Base-Tx,cat5 UTP
Data rate	10/100M
Forwarding rate	10 Mbps / 14,880 pps ,100 Mbps / 148,800 pps
LED Indicator	10/100Mbps(Link/Act),Power
Dimension	138*103*35mm
Power Input	DC5V/1000mA
Power Consumption	Max4.5W
Environment	Operating Temperature: 0 ℃-40 ℃
	Relative Humidity: 10%-90%(non-condensing)
	Storage Temperature: -40℃-70℃
	Relative Humidity: 5%-90%(non-condensing)

Chipset Feature :

- Built in 8 internal PHY, 8 SS-SMII (SMII), and one MII
- Built in 1.625Mb RAM
- Support packet length up to 1600 Bytes
- Store & forward, share memory, non-blocking architecture

- Support flow control
  - 802.3x in full duplex
  - Collision/Carrier_sense based backpressure in half duplex

- Provide up to 4K MAC address entries
  - CRC/ direct hashing algorithm
  - Programmable aging timer (55s~1812070.4s)

  - Wire speed address learning and resolution
  - CPU accessible for security and static MAC
  - Learning enable/disable
  - IP filter

- Support Sniffer function (in, out, in & out)

- Support IGMP snooping function Version 1,2
  - Support up to 2 trunk groups
  - (Port 0~3, port 4~7)

  - Load balance based on (port, DA, SA, DA / SA)

- Support VLAN
  - Port based VLAN
  - Tag based VLAN based on Ports & VIDs

  - Add/ remove/ modify tag
- Support Class of Service
  - Port based CoS function
  - 802.1Q priority tag based
  - IP TOS based (IPv4/IPv6)
  - TCP/UDP port based
  - 4 queues for per port
  - WRR/ FIFS/ SP algorithm
- Broadcast storm control support
  - Broadcast rate control per port
  - Block broadcast packet that not belongs to ARP or IPv4 packet to CPU port
- Support port security
  - MAC address based
  - IP address based
- Supports Bandwidth control
  - 255 configurable levels for P0~P16, (from 32kbps to 7.96 Mbps) for low bandwidth
  - 255 configurable levels for P0-P16 (from 512kbps to 100 Mbps) for high bandwidth
  - With/without flow control
- Support SMI auto-polling function
  - Poll for speed, duplex, flow control, and link
  - CPU accessible (interrupt support)
- CPU R/W PHY registers
- Support SS_SMII and SMII mode
- Support 4 port states for Spanning Tree protocol
  - Discarding/Blocking/learning/ forwarding
  - Forward BPDU to CPU port

- Captures specific packet to CPU port
- BPDU, LACP, 802.1X, GMRP, GVRP, ARP

- ICMP, IGMP, TCP, UDP, OSPF, other IP protocols
  - Packets with specific TCP/UDP port number

- Flexible PHY address setting for CPU

- Support three Configuration modes
  - Pin initial setting

  - 2 wire serial interface for EEPROM
  - 2 wire serial interface for CPU
- Statistic counters for each port
  - RX/TX packet count
  - CRC error packet count
  - Drop packet count
  - Collision count

- Support force link without SMI for Port16
- Support Non association port
- Support port based address flush

- Support LED functions (for p0~p7)
  - Support 2 bit serial,3 bit serial, and 3 bit bi color mode
  - Support direct LED mode for Link/Activity, speed, duplex states
  - Support bi color direct LED mode

- Only one 25MHz crystal is needed
- Adjustable IO voltage (3.3v MII1.95V SS-SMII)
- Programmable MAC address table through CPU interface
- 128 pin PQFP Lead free package

4、LED State

LED	Color	10M	100M	1G
Link	Green	ON	ON	ON
Action	Green	Twinkle	Twinkle	Twinkle